REMARKS

Applicants note with appreciation the opportunity granted by the Examiner to discuss the pending claims and the applied references. Now in the application are claims 1-36, of which claims 1, 14, 21, 25, 29, 33-36 are independent. No new matter has been entered and no new issues are raised. The following comments address all stated grounds of rejection, and place the presently pending claims, as identified above, in condition for allowance.

Claim Rejections under 35 U.S.C. §103

Claims 1-36 stand rejected under 35 U.S.C. §103. For clarity in the discussion below each respective claim set is discussed separately.

I. Rejection of Claims 1-13 under 35 U.S.C. §103(a);

Claims 1-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the publication entitled "Composable Models for Simulation-Based Design" by Paredis *et al.* (hereinafter "Paredis") in view of a user manual for System View by Elanix® (hereinafter "System View"). Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of these claims.

Claims 2-13 depend, directly or indirectly, upon independent claim 1, and therefore incorporate the patentable features of claim 1.

Claim 1 is directed toward a modeling process. The modeling process provides a plurality of blocks with each of the blocks representing functional entities. The modeling process generates a plurality of output signal values from the plurality of blocks, and groups the plurality of output signal values as an ordered set in a multiplexer as a first composite signal. In turn, the modeling process outputs the first composite signal.

Neither Paredis nor System View, alone or in combination, detracts from the patentability of claim 1. More specifically, Paredis, *inter alia*, teaches a hierarchically defined port-based modeling system and System View teaches a dynamic systems analysis environment for the design and simulation of engineering or scientific systems. Nevertheless, neither Paredis nor System View, alone or in combination, teach a modeling process that includes, among other steps, a step of grouping a plurality of output signals as an ordered set in a multiplexer as a first composite signal.

In contrast to claim 1, on page 272 of the System View reference is representation of a system model suitable for use as a 16-QAM constellation generator. The representation includes an I-channel and a Q-channel, which feed a first input port and a second input port, respectively, of an adder block. According to the System View function library included in the System View reference the adder block can perform complex addition. For example, the output signal of the adder block depicted on page 272 can be represented mathematically as $Y(t) = I_k\cos(2\pi f_c t) + Q_k\sin(2\pi f_c t)$. That is, the adder block taught by System View does not group a plurality of output signal values as an ordered set. Applicants further contend that the remainder of the System View reference is free of any such teaching. As such, Applicants contend neither Paredis nor System View, alone or in combination, teach a step of grouping of plurality of output signal as an ordered set in multiplexer as a first composite signal.

Hence, neither Paredis nor System View, alone or in combination, detract from the patentability of claims 1-13. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claims 1-13 under 35 U.S.C. §103.

II. Rejection of Claims 14-20 under 35 U.S.C. §103(a);

Claims 14-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paredis in view of System View. Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of these claims.

Claims 15-20 depend, directly or indirectly, upon independent claim 14, and therefore incorporate the patentable features of claim 14.

Claim 14 is directed to a block diagram modeling process that includes, among other steps, a step of grouping a plurality of output signal values as an ordered set in a multiplexer as a first composite signal. Applicants respectfully contend neither Paredis nor System View, alone or in combination, teach or suggest such a step.

Neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 14. As discussed above in relation to the rejection of Claims 1-13, the System View reference teaches an example of complex addition and does not teach formation of an ordered set by grouping of a plurality of output signals. More specifically, the adder block taught by system view is capable of performing an addition operation that adds two complex values and output the result. The adder block taught by System View does not group a plurality of output signal values as an ordered set in a multiplexer as a first composite signal. Paredis does not bridge the factual deficiencies of System View because Paredis, like System View, does not teach or suggest grouping a plurality of output signal values as an ordered set in a multiplexer in a first composite signal. As such, Applicants contend neither Paredis nor System View, alone or in combination, detract from the patentability of Claims 14-20.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 14-20 under 35 U.S.C. § 103.

III. Rejection of Claims 21-24 under 35 U.S.C. §103(a);

Claims 21-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paredis in view of System View. Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of these claims.

Claims 22-24 depend, directly or indirectly, upon independent claim 21, and therefore incorporate the patentable features of claim 21.

Claim 21 is directed to a computer program product residing on a computer-readable medium having instructions stored thereon, which, when executed, i.e., by a processor, causes the processor, among other actions, to group a plurality of output signal values as an ordered set in a multiplexer as a first composite signal. Applicants respectfully contend neither Paredis nor System View, alone or in combination, teach or suggest such an act, and therefore, do not detract from the patentability of claims 21-24.

Neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 21. As discussed above in relation to the rejection of Claims 1-13, the System View reference teaches an example of complex addition and does not teach formation of an ordered set by grouping of a plurality of output signals. More specifically, the adder block taught by system view is capable of performing an addition operation that adds two complex values and output the result. The adder block taught by System View does not group a plurality of output signal values as an ordered set in a multiplexer as a first composite signal. Paredis does not bridge the factual deficiencies of System View because Paredis, like System View, does not teach or suggest grouping a plurality of output signal values as an ordered set in a multiplexer in a first composite signal. As such, Applicants contend neither Paredis nor System View, alone or in combination, detract from the patentability of Claims 21-24.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 21-24 under 35 U.S.C. § 103.

IV. Rejection of Claims 25-28 under 35 U.S.C. §103(a);

Claims 25-28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paredis in view of System View. Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of these claims.

Claims 26-28 depend, directly or indirectly, upon independent claim 25, and therefore incorporate the patentable features of claim 25.

Claim 25 is directed to a processor and a memory configured to group a plurality of output signals as an ordered set in a multiplexer as a first composite signal. Applicants respectfully contend that neither Paredis nor System View, alone or in combination, teach or suggest such a processor and a memory, and therefore, do not detract from the patentability of claims 25-28.

Neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 25. As discussed above in relation to the rejection of Claims 1-13, the System View reference teaches an example of complex addition and does not teach formation of an ordered set by grouping of a plurality of output signals. More specifically, the adder block taught by system view is capable of performing an addition operation that adds two complex values and output the result. The adder block taught by System View does not group a plurality of output signal values as an ordered set in a multiplexer as a first composite signal. Paredis does not bridge the factual deficiencies of System View because Paredis, like System View, does not teach or suggest grouping a plurality of output signal values as an ordered set in a multiplexer in a first composite signal. As such, Applicants contend neither

Paredis nor System View, alone or in combination, detract from the patentability of Claims 25-28.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 25-28 under 35 U.S.C. § 103.

V. Rejection of Claims 29-32 under 35 U.S.C. §103(a);

Claims 29-32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paredis in view of System View. Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of these claims.

Claims 30-32 depend, directly or indirectly, upon independent claim 29, and therefore incorporate the patentable features of claim 29.

Claim 29 is directed to a modeling process that includes the steps of providing a plurality of blocks, grouping output signals from the blocks as an ordered set in a multiplexer as a composite signal, and outputting the composite signal. Neither Paredis nor System View, alone or in combination, teach or suggest such a modeling process, and therefore, do not detract from the patentability of the claims 29-32.

Neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 29. As discussed above in relation to the rejection of Claims 1-13, the System View reference teaches an example of complex addition and does not teach formation of an ordered set by grouping output signals. More specifically, the adder block taught by system view is capable of performing an addition operation that adds two complex values and output the result. The adder block taught by System View does not group output signals as an ordered set in a multiplexer as a composite signal. Paredis does not bridge the factual deficiencies of System View because Paredis, like System View, does not teach or suggest

grouping output signals as an ordered set in a multiplexer as a composite signal. As such, Applicants contend neither Paredis nor System View, alone or in combination, detract from the patentability of Claims 29-32.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 29-32 under 35 U.S.C. § 103.

VI. Rejection of Claim 33 under 35 U.S.C. §103(a);

Claim 33 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Paredis in view of System View. Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of this claim.

Claim 33 is directed to a computer program product residing on a computer-readable medium having instructions stored thereon, which, when executed by a processor cause the processor to group output signals from one or more blocks as an ordered set in a multiplexer as a composite signal and output the composite signal. Neither Paredis nor System View, alone or in combination, teach or suggest such a computer program product, and therefore, do not detract from the patentability of Claim 33.

Neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 33. As discussed above in relation to the rejection of Claims 1-13, the System View reference teaches an example of complex addition and does not teach formation of an ordered set by grouping output signals. More specifically, the adder block taught by system view is capable of performing an addition operation that adds two complex values and output the result. The adder block taught by System View does not group output signals as an ordered set in a multiplexer as a composite signal. Paredis does not bridge the factual deficiencies of System View because Paredis, like System View, does not teach or suggest

grouping output signals as an ordered set in a multiplexer as a composite signal. As such, Applicants contend neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 33.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 33 under 35 U.S.C. § 103.

VII. Rejection of Claim 34 under 35 U.S.C. §103(a);

Claim 34 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Paredis in view of System View. Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of this claim.

Claim 34 is directed to a processor and memory configured to provide a number of blocks, group the output signals of the blocks as an ordered set in a multiplexer as a complex signal, and output the composite signal. Neither Paredis nor System View, alone or in combination, teach or suggest such a processor and memory, and therefore, do not detract from the patentability of Claim 34.

Neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 34. As discussed above in relation to the rejection of Claims 1-13, the System View reference teaches an example of complex addition and does not teach formation of an ordered set by grouping output signals. More specifically, the adder block taught by system view is capable of performing an addition operation that adds two complex values and output the result. The adder block taught by System View does not group output signals as an ordered set in a multiplexer as a composite signal. Paredis does not bridge the factual deficiencies of System View because Paredis, like System View, does not teach or suggest grouping output signals as an ordered set in a multiplexer as a composite signal. As such,

Applicants contend neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 34.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 34 under 35 U.S.C. § 103.

VIII. Rejection of Claim 35 under 35 U.S.C. §103(a);

Claim 35 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Paredis in view of System View. Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of this claim.

Independent Claim 35 is directed towards a method for providing a composite signal in a modeling environment. The claim includes the steps of providing a plurality of output signals from one or more blocks, generating a *composite signal comprising a set of the plurality of output signals*, and providing the composite signal as an output signal. Neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 35.

As discussed above in relation to the rejection of Claims 1-13, the System View reference teaches an example of complex addition and does not teach generation of a composite signal that includes a set of output signals. More specifically, the adder block taught by system view is capable of performing an addition operation that adds two complex values and output the result. The adder block taught by System View does not generate a composite signal that includes a set of output signals. Paredis does not bridge the factual deficiencies of System View because Paredis, like System View, does not teach or suggest generation of a composite signal that includes a set of the output signals. As such, Applicants contend neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 35.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 35 under 35 U.S.C. § 103.

VIX. Rejection of Claim 36 under 35 U.S.C. §103(a);

Claim 36 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Paredis in view of System View. Applicants respectfully traverse this rejection and contend that neither Paredis nor System View, alone or in combination, teach or suggest each and every element of this claim.

Independent Claim 36 is directed towards a method for graphically representing a composite signal in a modeling environment. The claim includes the step of providing a plurality of output signals from one or more blocks and each output signal is graphically indicated by a signal identifier. The claim further includes the step of *providing a composite signal identifier to graphically indicate a grouping of signal identifiers.* The composite signal identifier represents a composite signal comprising a set of the plurality of output signals. Neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 36.

As discussed above in relation to the rejection of Claims 1-13, the System View reference teaches an example of complex addition and does not teach providing a composite signal identifier to graphically indicate a grouping of signal identifiers. More specifically, the adder block taught by system view is capable of performing an addition operation that adds two complex values and output the result. The adder block taught by System View does not provide a composite signal identifier to graphically indicate a grouping of signal identifiers. Paredis does not bridge the factual deficiencies of System View because Paredis, like System View, does not teach or suggest providing a composite signal identifier to graphically

indicate a grouping of signal identifiers. As such, Applicants contend neither Paredis nor System View, alone or in combination, detract from the patentability of Claim 36.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 36 under 35 U.S.C. § 103.

CONCLUSION

In view of the remarks set forth above, Applicants contend each of the presently pending claims in this application is in immediate condition for allowance. Accordingly, Applicants respectfully request the Examiner to pass the claims to allowance.

If the Examiner deems there are any remaining issues, we invite the Examiner to call the Applicants' Attorney at the telephone number identified below.

Respectfully submitted,
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Dated: June 10, 2005

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